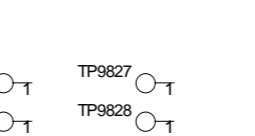
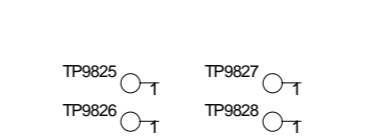
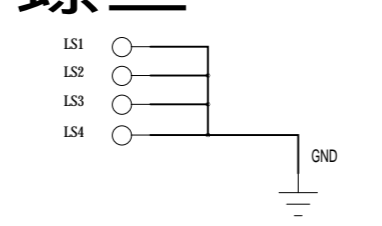
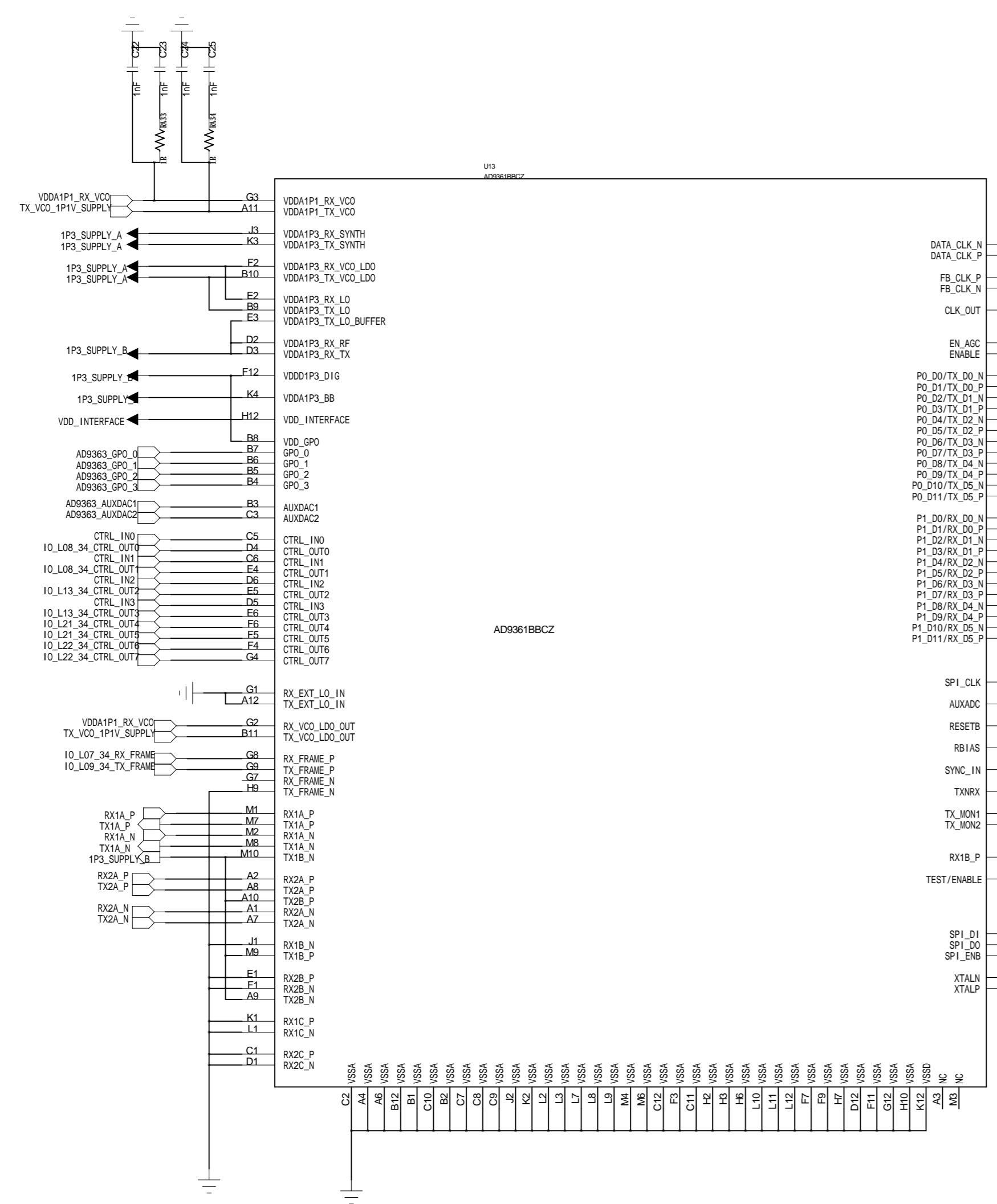
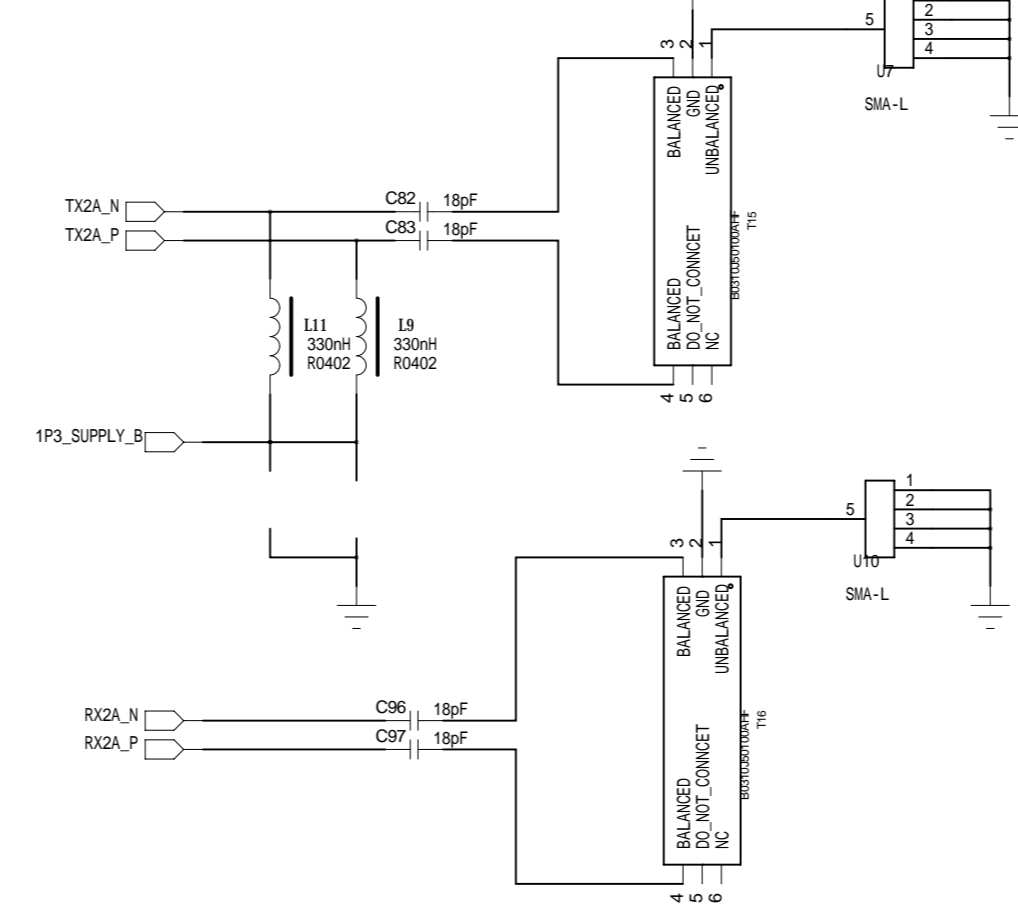
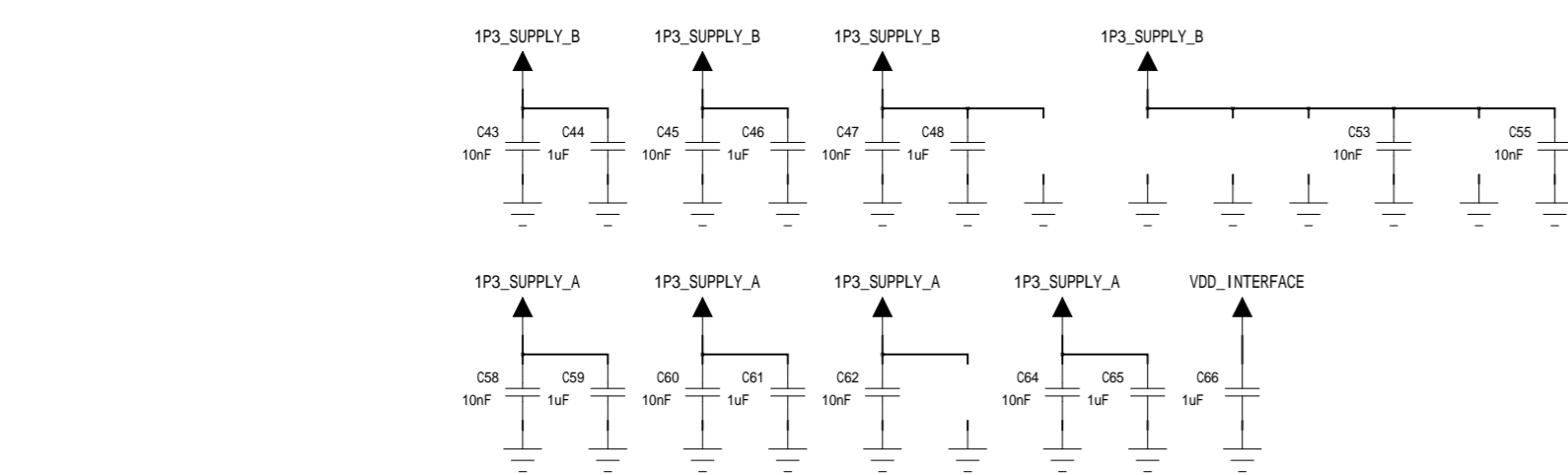


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DATA_CLK_N	H11	IO_L12_MRCC_34_DATA_CLK
DATA_CLK_P	G11	IO_L12_MRCC_34_DATA_CLK
FB_CLK_P	F10	IO_L01_34_FB_CLK
FB_CLK_N	G10	IO_L01_34_FB_CLK
CLK_OUT	J5	IO_02_34_AD9361_CLKOUT
EN_AGC	G5	IO_L10_34_EN_AGC
ENABLE	G6	IO_L11_34_ENABLE
PD_D0_TX_D0_N	E12	IO_L15_34_TX_D0
PD_D1_TX_D0_P	D11	IO_L15_34_TX_D1
PD_D2_TX_D1_N	E11	IO_L15_34_TX_D2
PD_D3_TX_D1_P	D10	IO_L15_34_TX_D3
PD_D4_TX_D2_N	E10	IO_L17_34_TX_D4
PD_D5_TX_D2_P	D9	IO_L17_34_TX_D5
PD_D6_TX_D3_N	E9	IO_L18_34_TX_D6
PD_D7_TX_D3_P	D8	IO_L18_34_TX_D7
PD_D8_TX_D4_N	E8	IO_L18_34_TX_D8
PD_D9_TX_D4_P	D7	IO_L18_34_TX_D9
PD_D10_TX_D5_N	E7	IO_L20_34_TX_D10
PD_D11_TX_D5_P	D6	IO_L20_34_TX_D11
PI_D0/RX_D0_N	K11	IO_L01_34_RX_D0
PI_D1/RX_D0_P	J12	IO_L01_34_RX_D1
PI_D2/RX_D1_N	K10	IO_L02_34_RX_D2
PI_D3/RX_D1_P	J11	IO_L02_34_RX_D3
PI_D4/RX_D2_N	K9	IO_L03_34_RX_D4
PI_D5/RX_D2_P	J10	IO_L03_34_RX_D5
PI_D6/RX_D3_N	K8	IO_L04_34_RX_D6
PI_D7/RX_D3_P	J9	IO_L04_34_RX_D7
PI_D8/RX_D4_N	K7	IO_L05_34_RX_D8
PI_D9/RX_D4_P	J8	IO_L05_34_RX_D9
PI_D10/RX_D5_N	K6	IO_L06_34_RX_D10
PI_D11/RX_D5_P	J7	IO_L06_34_RX_D11
SPI_CLK	J5	IO_L23_35_SPI_CLK
AUXADC	L5	AD9361_AUXADC
RESETB	K5	IO_02_34_AD9361_RST
FB1A0	L4	10.1K
SYNC_IN	H5	
TNRX	H4	IO_L11_34_TNRX
TX_MON1	M5	
TX_MON2	M6	
RX1B_P	H1	
RX1B_N	C4	
TEST/ENABLE		
SPI_D1	J4	IO_L24_35_SPI_D1
SPI_D0	L6	IO_L24_35_SPI_D0
SPI_ENB	K6	IO_L23_35_SPI_ENB
XTALN	M12	
XTALP	M11	

